CLAIMS

What is claimed is:

1. A process for forming a semiconductor structure comprising:
forming a gate dielectric overlying a substrate, a conductive gate electrode overlying the gate dielectric, a barrier layer overlying and in physical contact with the conductive gate electrode, and an organic anti-reflective coating (ARC) layer overlying and in physical contact with the barrier layer.

2. The process of claim 1, wherein forming comprises forming a masking layer overlying the organic ARC layer.

3. The process of claim 2, further comprising removing the masking layer and the organic ARC layer.

4. The process of claim 3, wherein forming comprises forming an oxygen-containing layer between the organic ARC layer and the masking layer, and wherein removing comprises removing the masking layer, the oxygen-containing layer, and the organic ARC layer.

5. The process of claim 3, further comprising removing the barrier layer.

6. The process of claim 1, wherein the conductive gate electrode comprises a metal.

7. The process of claim 6, wherein the barrier layer is further characterized as an oxygen resistant barrier layer.

8. The process of claim 6, wherein the barrier layer comprises at least one of silicon and nitrogen.

9. The process of claim 8, wherein the barrier layer comprises silicon and nitrogen.

10. The process of claim 6, wherein the barrier layer comprises a metal selected from a group consisting of iridium, ruthenium, and platinum.

11. The process of claim 6, wherein the barrier layer comprises a metal whose oxides are conductive.

12. The process of claim 6, wherein the barrier layer comprises amorphous silicon.

13. The process of claim 1, wherein the conductive gate electrode comprises polysilicon.

14. The process of claim 1, wherein the barrier layer has a thickness in a range of approximately 20 Angstroms to 500 Angstroms.

15. The process of claim 1, wherein the organic ARC layer comprises carbon.

16. A process for forming a semiconductor structure, comprising:
forming a gate dielectric layer overlying a substrate;
forming a metal gate electrode layer overlying the gate dielectric layer;
forming a barrier layer overlying the metal gate electrode layer;
forming a carbon-containing ARC layer overlying the barrier layer;
forming a patterned masking layer overlying the carbon-containing ARC layer; and
removing portions of the gate dielectric layer, the metal gate electrode layer, the barrier layer, and the carbon-containing ARC layer using the patterned masking layer to form an intermediate gate stack.

17. The process of claim 16, further comprising:
removing the masking layer and the carbon-containing ARC layer from the intermediate gate stack to form a gate stack.

18. The process of claim 17, wherein removing the masking layer and the carbon-containing ARC layer is performed in an oxygen and plasma environment.

19. The process of claim 18, wherein during removal of the masking layer and the carbon-containing ARC layer in the oxygen and plasma environment, the barrier layer retards oxygen from diffusing into the metal gate electrode layer of the intermediate gate stack.

20. The process of claim 18, further comprising:
forming spacers adjacent to each sidewall of the gate stack;
forming source and drain regions in the substrate, underlying at least a portion of the spacers and the gate stack.

21. The process of claim 20, further comprising:
removing the barrier layer from the gate stack; and
saliciding the source and drain regions.

22. The process of claim 21, wherein removing the barrier layer is performed after saliciding the source and drain regions.

23. The process of claim 16, wherein the barrier layer is characterized as one of an oxygen resistant and an oxygen absorbing layer.

24. The process of claim 16, wherein the barrier layer comprises at least one of silicon and nitrogen.

25. The process of claim 16, wherein the barrier layer comprises at least one selected from the group consisting of a non-conductive oxygen resistant layer, a conductive oxygen resistant layer, and a conductive oxygen absorbing layer.

26. The process of claim 16, wherein the barrier layer is in direct physical contact with the metal gate electrode layer, and the carbon-containing ARC layer is in direct physical contact with the barrier layer.

27. The process of claim 26, wherein the barrier layer has a thickness in a range of approximately 20 Angstroms to 500 Angstroms.

28. The processing of claim 16, further comprising forming an oxygen-containing layer overlying the carbon-containing ARC layer, wherein the pattern masking layer is formed overlying the oxygen-containing layer, and wherein removing further comprises removing portions of the oxygen-containing layer to form the intermediate gate stack.

29. A semiconductor structure, comprising:
a gate dielectric overlying a substrate;
a metal gate electrode overlying the gate dielectric; and
an oxygen diffusion barrier layer overlying and in physical contact with the conductive gate electrode.

30. The semiconductor structure of claim 29, wherein the oxygen diffusion barrier layer comprises at least one of silicon and nitrogen.

31. The semiconductor structure of claim 29, wherein the barrier layer comprises at least one selected from the group consisting of a non-conductive oxygen resistant layer, a conductive oxygen resistant layer, and a conductive oxygen absorbing layer.

32. The semiconductor structure of claim 29, wherein the oxygen diffusion barrier layer comprises amorphous silicon.